

Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding a ball bond connection joint are disclosed in U.S. Application Serial No. 09/864,773 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Ball Bond Connection Joint" which is incorporated by reference. Further details regarding a solder or conductive adhesive connection joint are disclosed in U.S. Application Serial No. 09/927,216 filed August 10, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Hardened Connection Joint" which is incorporated by reference.

Replace the paragraph at page 32, lines 18-22 with the following paragraph:

For instance, if an optoelectronic chip is employed with a light sensitive cell and pads on the upper surface, the pads, adhesive, conductive traces and connection joints are disposed outside the light sensitive cell, and the insulative base is a transparent epoxy layer that is deposited on the light sensitive cell, then the light sensitive cell will receive light from the external environment that impinges upon and passes through the insulative base.

In the Claims

Cancel claims 61-140 without prejudice or disclaimer to the subject matter recited therein.

Add the following claims:

- 1 141. A method of making a semiconductor package device, comprising:
 - 2 attaching a semiconductor chip to a metallic structure using an insulative adhesive,
 - 3 wherein the chip includes a conductive pad, the metallic structure includes first and second
 - 4 opposing surfaces and a conductive trace, the adhesive is disposed between the first surface and
 - 5 the chip, the conductive trace includes a recessed portion, a non-recessed portion and opposing
 - 6 outer edges between the first and second surfaces that extend across the recessed and non-
 - 7 recessed portions, and the recessed portion is recessed relative to the non-recessed portion at the
 - 8 second surface;

9 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
10 recessed portion, wherein the encapsulant covers the chip, the outer edges and the recessed
11 portion, and the non-recessed portion extends outside the encapsulant; and
12 forming a connection joint that electrically connects the conductive trace and the pad.

1 142. The method of claim 141, wherein the recessed portion is located between the
2 non-recessed portion and the chip.

1 143. The method of claim 141, wherein the recessed portion is formed by etching the
2 metallic structure.

1 144. The method of claim 141, whercin the reccessed portion is coplanar with the non-
2 recessed portion at the first surface.

1 145. The method of claim 141, wherein the recessed portion is coplanar with the non-
2 recessed portion at the outer edges.

1 146. The method of claim 141, wherein the recessed portion is coplanar with the non-
2 recessed portion at the first surface and the outer edges.

1 147. The method of claim 141, wherein the outer edges are defined by first and second
2 slots in the metallic structure.

1 148. The method of claim 141, wherein the outer edges are formed by etching the
2 metallic structure.

1 149. The method of claim 141, wherein the outer edges are formed by simultaneously
2 etching the first and second surfaces.

1 150. The method of claim 141, wherein the metallic structure is a copper lead frame.

1 151. The method of claim 141, wherein the adhesive is the only insulator that contacts
2 and is attached to the metallic structure before forming the encapsulant.

1 152. The method of claim 141, wherein the adhesive contacts the pad.

1 153. The method of claim 141, wherein the adhesive is spaced from a side of the chip
2 opposite the pad.

1 154. The method of claim 141, wherein the adhesive is spaced from the second surface.

1 155. The method of claim 141, wherein the encapsulant is coplanar with the non-
2 recessed portion at the second surface.

1 156. The method of claim 141, wherein the encapsulant contacts substantially none of
2 the non-recessed portion at the second surface.

1 157. The method of claim 141, wherein the encapsulant contacts an entire side of the
2 chip opposite the pad.

1 158. The method of claim 141, wherein the encapsulant is formed by transfer molding.

1 159. The method of claim 141, wherein the steps are performed in the sequence set
2 forth.

1 160. The method of claim 141, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

1 161. A method of making a semiconductor package device, comprising:
2 providing a metallic structure that includes first and second opposing surfaces, wherein
3 the metallic structure further includes a conductive trace and a pair of slots, the conductive trace
4 includes a recessed portion, a non-recessed portion and opposing outer edges defined by the slots
5 that are parallel to one another, extend between the first and second surfaces and extend across

6 the recessed and non-recessed portions, and the recessed portion is adjacent to the non-recessed
7 portion, coplanar with the non-recessed portion at the first surface, recessed relative to the non-
8 recessed portion at the second surface and provides a channel between the slots;

9 attaching the metallic structure to a semiconductor chip that includes a conductive pad,
10 wherein the first surface faces towards the chip and the second surface faces away from the chip;

11 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
12 recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed
13 portion extends outside the encapsulant; and

14 forming a connection joint that contacts and electrically connects the conductive trace and
15 the pad.

1 162. The method of claim 161, including forming the recessed portion and partially
2 forming the slots by selectively etching the metallic structure from the second surface towards
3 the first surface.

1 163. The method of claim 162, including partially forming the slots by selectively
2 etching the metallic structure from the first surface towards the second surface.

1 164. The method of claim 161, including removing the encapsulant from portions of
2 the slots adjacent to the non-recessed portion without removing the encapsulant from the
3 channel.

1 165. The method of claim 161, wherein the encapsulant contacts an entire side of the
2 chip opposite the pad.

1 166. The method of claim 161, wherein the encapsulant is coplanar with the non-
2 recessed portion at the second surface.

1 167. The method of claim 161, wherein the encapsulant contacts substantially none of
2 the non-recessed portion at the second surface.

1 168. The method of claim 161, wherein the encapsulant is formed by transfer molding.

1 169. The method of claim 161, wherein the steps are performed in the sequence set
2 forth.

1 170. The method of claim 161, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

1 171. A method of making a semiconductor package device, comprising:
2 providing a metallic structure that includes first and second opposing surfaces;
3 selectively etching the metallic structure to form a pair of slots that extend between the
4 first and second surfaces and a recessed portion that extends into the metallic structure at the
5 second surface towards the first surface and extends between the slots, wherein the metallic
6 structure further includes a non-recessed portion that extends between the slots, the recessed
7 portion is adjacent to the non-recessed portion, coplanar with the non-recessed portion at the first
8 surface, recessed relative to the non-recessed portion at the second surface and provides a
9 channel between the slots, and the slots define opposing outer edges that are parallel to one
10 another, extend between the first and second surfaces and extend across the recessed and non-
11 recessed portions;

12 attaching the metallic structure to a semiconductor chip using an insulative adhesive,
13 wherein the chip includes a conductive pad, the first surface faces towards the chip, the second
14 surface faces away from the chip, and the recessed portion is located between the chip and the
15 non-recessed portion;

16 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
17 recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed
18 portion extends outside the encapsulant; and

19 forming a connection joint that contacts and electrically connects the metallic structure
20 and the pad.

1 172. The method of claim 171, including forming the recessed portion and partially
2 forming the slots by selectively etching the metallic structure from the second surface towards
3 the first surface.

1 173. The method of claim 172, including partially forming the slots by selectively
2 etching the metallic structure from the first surface towards the second surface.

1 174. The method of claim 171, including removing the encapsulant from portions of
2 the slots adjacent to the non-recessed portion without removing the encapsulant from the
3 channel.

1 175. The method of claim 171, wherein the encapsulant contacts an entire side of the
2 chip opposite the pad.

1 176. The method of claim 171, wherein the encapsulant is coplanar with the non-
2 recessed portion at the second surface.

1 177. The method of claim 171, wherein the encapsulant contacts substantially none of
2 the non-recessed portion at the second surface.

1 178. The method of claim 171, wherein the encapsulant is formed by transfer molding.

1 179. The method of claim 171, wherein the steps are performed in the sequence set
2 forth.

1 180. The method of claim 171, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

1 181. A method of making a semiconductor package device, comprising:
2 providing a metallic structure that includes first and second opposing surfaces, wherein
3 the metallic structure further includes a conductive trace and a pair of slots, the conductive trace
4 includes a recessed portion, a non-recessed portion and opposing outer edges defined by the slots
5 that are parallel to one another, extend between the first and second surfaces and extend across
6 the recessed and non-recessed portions, and the recessed portion is adjacent to the non-recessed

7 portion, coplanar with the non-recessed portion at the first surface, recessed relative to the non-
8 recessed portion at the second surface and provides a channel between the slots;

9 depositing a metal trace on the metallic structure, wherein the metal trace includes a
10 terminal that extends into the metallic structure at the first surface and a routing line that contacts
11 the recessed portion at the first surface;

12 attaching the metallic structure to a semiconductor chip that includes a conductive pad,
13 wherein the first surface faces towards the chip, the second surface faces away from the chip, the
14 pad faces towards the first surface, the routing line extends within and outside a periphery of the
15 chip, and the recessed and non-recessed portions are located outside the periphery of the chip;

16 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
17 recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed
18 portion extends outside the encapsulant; and

19 forming a connection joint that contacts and electrically connects the conductive trace and
20 the pad.

1 182. The method of claim 181, including forming the recessed portion and partially
2 forming the slots by selectively etching the metallic structure from the second surface towards
3 the first surface.

1 183. The method of claim 182, including partially forming the slots by selectively
2 etching the metallic structure from the first surface towards the second surface.

1 184. The method of claim 181, including removing the encapsulant from portions of
2 the slots adjacent to the non-recessed portion without removing the encapsulant from the
3 channel.

1 185. The method of claim 181, wherein the encapsulant contacts an entire side of the
2 chip opposite the pad.

1 186. The method of claim 181, wherein the encapsulant is coplanar with the non-
2 recessed portion at the second surface.

1 187. The method of claim 181, wherein the encapsulant contacts substantially none of
2 the non-recessed portion at the second surface.

1 188. The method of claim 181, whercin the encapsulant is formed by transfer molding.

1 189. The method of claim 181, wherein the steps are performed in the sequence set
2 forth.

1 190. The method of claim 181, whercin the device is devoid of wire bonds, TAB leads
2 and solder joints.

1 191. A method of making a semiconductor package device, comprising:
2 providing a metallic structure that includes first and second opposing surfaces;
3 selectively etching the metallic structure to form a pair of slots that extend between the
4 first and second surfaces and a recessed portion that extends into the metallic structure at the
5 second surface towards the first surface and extends between the slots, wherein the metallic
6 structure further includes a non-recessed portion that extends between the slots, the recessed
7 portion is adjacent to the non-recessed portion, coplanar with the non-recessed portion at the first
8 surface, recessed relative to the non-recessed portion at the second surface and provides a
9 channel between the slots, and the slots define opposing outer edges that are parallel to one
10 another, extend between the first and second surfaces and extend across the recessed and non-
11 recessed portions;

12 depositing a metal trace on the metallic structure, wherein the metal trace includes a
13 terminal that extends into the metallic structure at the first surface and a routing line that contacts
14 the recessed portion at the first surface;

15 attaching the metallic structure to a semiconductor chip using an insulative adhesive,
16 wherein the chip includes a conductive pad, the first surface faces towards the chip, the second
17 surface faces away from the chip, the pad faces towards the first surface, the routing line extends
18 within and outside a periphery of the chip, the recessed and non-recessed portions are located

19 outside the periphery of the chip and the recessed portion is located between the chip and the
20 non-recessed portion;

21 forming an encapsulant that contacts the chip, the first surface, the outer edges and the
22 recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed
23 portion extends outside the encapsulant; and

24 forming a connection joint that contacts and electrically connects the metallic structure
25 and the pad.

1 192. The method of claim 191, including forming the recessed portion and partially
2 forming the slots by selectively etching the metallic structure from the second surface towards
3 the first surface.

1 193. The method of claim 192, including partially forming the slots by selectively
2 etching the metallic structure from the first surface towards the second surface.

1 194. The method of claim 191, including removing the encapsulant from portions of
2 the slots adjacent to the non-recessed portion without removing the encapsulant from the
3 channel.

1 195. The method of claim 191, wherein the encapsulant contacts an entire side of the
2 chip opposite the pad.

1 196. The method of claim 191, wherein the encapsulant is coplanar with the non-
2 recessed portion at the second surface.

1 197. The method of claim 191, wherein the encapsulant contacts substantially none of
2 the non-recessed portion at the second surface.

1 198. The method of claim 191, wherein the encapsulant is formed by transfer molding.

1 199. The method of claim 191, wherein the steps are performed in the sequence set
2 forth.

1 200. The method of claim 191, wherin the device is devoid of wire bonds, TAB leads
2 and solder joints.

1 201. A method of making a semiconductor package device, comprising:
2 providing a metal base that includes first and second opposing surfaces, wherin the
3 metal base further includes a pair of slots that extend between the first and second surfaces, a
4 first recessed portion that is recessed at the first surface and extends into the metal base towards
5 the second surface and is spaced from the slots, a second recessed portion that is recessed at the
6 second surface and extends into the metal base towards the first surface and is between and
7 adjacent to the slots and provides a channel between the slots, and a non-recessed portion that is
8 spaced from the first recessed portion, adjacent to the second recessed portion and between and
9 adjacent to the slots, wherein the first recessed portion is recessed relative to the non-recessed
10 portion at the first surface and coplanar with the non-recessed portion at the second surface, the
11 second recessed portion is coplanar with the non-recessed portion at the first surface and recessed
12 relative to the non-recessed portion at the second surface, and the second recessed portion and
13 the non-recessed portion form a lead between the slots;

14 depositing a metal trace on the metal base, wherein the metal trace includes a terminal in
15 the first recessed portion and a routing line on the first surface that contacts the lead;

16 attaching the metal base to a semiconductor chip using an insulative adhesive, wherein
17 the chip includes a conductive pad, the first surface faces towards the chip, the second surface
18 faces away from the chip, the terminal is between the pad and the second recessed portion, and
19 the second recessed portion is between the terminal and the non-recessed portion;

20 forming a first insulative housing portion that contacts the chip and fills the channel and
21 the slots without contacting the terminal;

22 etching the metal base, therby exposing the terminal and the adhesive;

23 forming a connection joint that contacts and electrically connects the routing line and the
24 pad; and

25 forming a second insulative housing portion that contacts the terminal and the adhesive,
26 wherein the terminal protrudes downwardly from and extends through the second insulative

27 housing portion, and the first and second insulative housing
28 portions form an insulative housing
that surrounds the chip.

1 202. The method of claim 201, wherein forming the slots and the recessed portions
2 includes:

3 forming a first etch mask on the first surface that includes openings that selectively
4 expose the first surface;

5 forming a second etch mask on the second surface that includes openings that selectively
6 expose the second surface;

7 applying a wet chemical etch through the openings in the first etch mask to selectively
8 etch the first surface, thereby forming the first recessed portion and partially forming the slots;

9 applying a wet chemical etch through the openings in the second etch mask to selectively
10 etch the second surface, thereby forming the second recessed portion and partially forming the
11 slots;

12 removing the first etch mask; and

13 removing the second etch mask.

1 203. The method of claim 202, including:

2 simultaneously forming the first and second etch masks;

3 simultaneously applying the wet chemical etches to the first and second surfaces; and

4 simultaneously removing the first and second etch masks.

1 204. The method of claim 201, wherein depositing the metal trace includes:

2 forming a plating mask on the first surface that includes an opening that selectively
3 exposes the first surface; and

4 electroplating the metal trace in the opening and on the exposed portion of the first
5 surface.

1 205. The method of claim 201, wherein etching the metal base to expose the terminal
2 and the adhesive includes:

3 depositing a protective coating on a portion of the lead that protrudes laterally from the
4 first insulative housing portion; and then

5 applying a wet chemical etch that is selective of the metal base with respect to the
6 protective coating.

1 206. The method of claim 205, wherein depositing the protective coating includes:
2 forming a plating mask on a portion of the second surface within a periphery of the first
3 insulative housing portion that selectively exposes the portion of the lead that protrudes laterally
4 from the first insulative housing portion; and

5 electroplating the protective coating on the portion of the lead that protrudes laterally
6 from the first insulative housing portion.

1 207. The method of claim 201, wherein forming the second insulative housing portion
2 includes:

3 depositing an insulative layer that covers the terminal; and
4 selectively removing a portion of the insulative layer that covers the terminal, thereby
5 exposing the terminal without exposing a portion of the routing line that contacts the lead.

1 208. The method of claim 201, wherein forming the second insulative housing portion
2 includes:

3 depositing an insulative layer that conformally covers the terminal; and
4 globally removing a surface portion of the insulative layer, thereby exposing the terminal
5 without exposing a portion of the routing line that contacts the lead.

1 209. The method of claim 201, wherein the steps are performed in the sequence set
2 forth.

1 210. The method of claim 201, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.

1 211. A method of making a semiconductor package device, comprising:
2 providing a metal base that includes first and second opposing surfaces;
3 etching the metal base to form a pair of slots that extend between the first and second
4 surfaces, a first recessed portion that is recessed at the first surface and extends into the metal
5 base towards the second surface and is spaced from the slots, and a second recessed portion that
6 is recessed at the second surface and extends into the metal base towards the first surface and is
7 between and adjacent to the slots and provides a channel between the slots, wherein the metal
8 base includes a non-recessed portion that is spaced from the first recessed portion, adjacent to the
9 second recessed portion and between and adjacent to the slots, the first recessed portion is
10 recessed relative to the non-recessed portion at the first surface and coplanar with the non-
11 recessed portion at the second surface, the second recessed portion is coplanar with the non-
12 recessed portion at the first surface and recessed relative to the non-recessed portion at the
13 second surface, and the second recessed portion and the non-recessed portion form a lead
14 between the slots;
15 depositing a metal trace on the metal base, wherein the metal trace includes a terminal in
16 the first recessed portion and a routing line on the first surface that contacts the lead;
17 attaching the metal base to a semiconductor chip using an insulative adhesive, wherein
18 the chip includes a conductive pad, the first surface faces towards the chip, the second surface
19 faces away from the chip, the terminal is between the pad and the second recessed portion, and
20 the second recessed portion is between the terminal and the non-recessed portion;
21 forming a first insulative housing portion that contacts the chip and fills the channel and
22 the slots without contacting the terminal;
23 removing the first insulative housing portion from a region of the slots, wherein the lead
24 protrudes laterally from and extends through the first insulative housing portion;
25 etching the metal base, thereby exposing the terminal and the adhesive;
26 forming an opening in the adhesive, thereby exposing the pad;
27 forming a connection joint that contacts and electrically connects the routing line and the
28 pad; and
29 forming a second insulative housing portion that contacts the terminal and the adhesive,
30 wherein the terminal protrudes downwardly from and extends through the second insulative

31 housing portion, and the first and second insulative housing portions form an insulative housing
32 that surrounds the chip.

1 212. The method of claim 211, whercin etching the metal base to form the slots and the
2 recessed portions includes:

3 forming a first etch mask on the first surface that includes openings that selectively
4 expose the first surface;

5 forming a second etch mask on the second surface that includes openings that selectively
6 expose the second surface;

7 applying a wet chemical etch through the openings in the first etch mask to selectively
8 etch the first surface, thereby forming the first recessed portion and partially forming the slots;

9 applying a wet chemical etch through the openings in the second etch mask to selectively
10 etch the second surface, thereby forming the second recessed portion and partially forming the
11 slots;

12 removing the first etch mask; and

13 removing the second etch mask.

1 213. The method of claim 212, including:

2 simultaneously forming the first and second etch masks;

3 simultaneously applying the wet chemical etches to the first and second surfaces; and

4 simultaneously removing the first and second etch masks.

1 214. The method of claim 211, wherein depositing the metal trace includes:

2 forming a plating mask on the first surface that includes an opening that selectcively
3 exposes the first surface; and

4 electroplating the metal trace in the opening and on the exposed portion of the first
5 surface.

1 215. The method of claim 211, wherein etching the metal base to expose the terminal

2 and the adhesive includes:

3 depositing a protective coating on a portion of the lead that protrudes laterally from the
4 first insulative housing portion; and then
5 applying a wet chemical etch that is selective of the metal base with respect to the
6 protective coating.

1 216. The method of claim 215, whercin depositing the protective coating includes:
2 forming a plating mask on a portion of the second surface within a periphery of the first
3 insulative housing portion that selectively exposes the portion of the lead that protrudes laterally
4 from the first insulative housing portion; and
5 electroplating the protective coating on the portion of the lead that protrudes laterally
6 from the first insulative housing portion.

1 217. The method of claim 211, whercin forming the second insulative housing portion
2 includes:
3 depositing an insulative layer that covers the terminal; and
4 selectively removing a portion of the insulative layer that covers the terminal, thereby
5 exposing the terminal without exposing a portion of the routing line that contacts the lead.

1 218. The method of claim 211, wherein forming the second insulative housing portion
2 includes:
3 depositing an insulative layer that conformally covers the terminal; and
4 globally removing a surface portion of the insulative layer, thereby exposing the terminal
5 without exposing a portion of the routing line that contacts the lead.

1 219. The method of claim 211, wherein the steps are performed in the sequence set
2 forth.

1 220. The method of claim 211, wherein the device is devoid of wire bonds, TAB leads
2 and solder joints.